IN THE SPECIFICATION

Please amend the paragraph starting on page 3, line 21 as indicated below:

The ~~program~~ programming algorithm 18 begins with the microprocessor coupled to the flash memory writing a program setup command (i.e., 40 Hexadecimal) to the command user interface of the flash memory followed by a second write operation that specifies the address and data. After successful receipt and interpretation of the requested program operation, the command user interface of the flash memory forwards a translated signal to the write state machine of the flash memory then takes over, controlling an internal program algorithm within the flash memory. In particular, the write state machine supervises internal program and verify circuits to perform the following tasks: (1) program pulse control, (2) pulse repetition control, (3) time-out control, (4) program verification, and (5) status register update.

Please amend the paragraph starting on page 11, line 20 as indicated below:

Figure 5 shows more details of flash nonvolatile memory 24. Flash memory 24 is comprised of a flash cell array 20, [[a]] command user interface circuitry 40, [[a]] write state machine 28, special programming mode circuitry 32, input/output logic 47, input buffers 51, 52, and 55, output buffers 53 and 54, output multiplexer 45, identifier register 85, status register 83, data register 91, data comparator 81, address input buffer 61, address latch 62, address counter 63, power reduction control circuitry 73, X decoder 71, Y decoder 72, program/erase voltage switch 41, and Y gating/sensing circuitry 74.

Please amend the paragraphs starting on page 12, line 12 as indicated below:

Control bus 106 is part of data lines 26 of FIG. 4. Data bus 104 is also part of lines 26 of FIG. 4. Address bus 102 is part of lines 26, also. Address bus 102, data bus 104, and control bus 106 couple the flash memory device 24 to host processor 22.

Flash memory device 24 has on-chip program and erase automation circuitry that includes the command user interface 40, write state machine 28, data comparator 81, and status register 83.

The command user interface circuitry 40 is a request interface for flash memory device 24. The basic job of the command user interface circuitry 40 is to arbitrate between host processor 22 and internal flash memory device 24 functions. The command user interface 40 serves this role via a command register to hold the issued request, a command decoder to interpret/translate that request, and the control logic to initiate action. Activities include communications between command user interface 40 and write state machine 28, read path selection, and status register 83 checking and clearing.

B3

Please amend the paragraph starting on page 16, line16 as indicated below:

If I_{PMRGN} is less than I_{PREF}, then the particular sense amplifier of sense amplifiers ~~117a-117p~~ 117A-117P outputs a logical one. This operation occurs for eight or sixteen bits in parallel, depending on the bus width of the program operation. The eight bit or sixteen bit output values from the sense amplifiers ~~117a-117p~~ 117A-117P are sent to the data comparator 81 for collation against data stored in data register 91.

B4

Please amend the paragraph starting on page 28, line 21 as indicated below:

The write state machine 28 and special programming mode circuitry 32 cause the read operation with respect to flash memory array 20 to occur at the program verification voltage levels. Thus, at process block 256, the write state machine 28 and special programming mode circuitry 32 cause a margined-sensing scheme to be used. An elevated read voltage is applied to the programmed cells. The current I_{PMRGN}, derived from a programmed margin bias read of the column containing the programmed cell, is fed into one of the sense amplifiers ~~117a-117p~~ 117A-117P with reference current I_{PREF}, which is the current from the factory set program reference circuit 111. If I_{PMRGN} is less than I_{PREF}, then the particular sense amplifier of sense amplifiers ~~117a-117p~~ 117A-117P outputs a zero. If I_{PMRGN} is greater than I_{PREF}, then sense amplifiers ~~117a-117p~~ 117A-117P outputs a logical one. These operations occur for all the bits of the word in parallel, using each of the sense amplifiers ~~117a-117p~~ 117A-117P.

B5

Please amend the paragraphs on page 37 starting at line 13 as indicated below:

For operations or procedures 320, there is a hash operation associated with each data word rather than a verification associated with the reading of each data word. At the end of the programming of the data stream, there is a single verification step involving the comparison of hash values.

B6

As shown in Figure 10, the program flow or procedures 320 starts at process block 322. At process block 322, flash memory array 24 enters the special programming mode. Thus flash memory array 24 enters the special programming mode state 152 by the host processor sending in a special programming command to flash memory device 24.

Please amend the paragraph on page 40 starting at line 1 as indicated below:

The process flow then moves to process block 354. At process block 354, the host processor 22 compares the hash value stored in flash memory array 20 with a hash value that the host processor 22 had stored in memory 34 to see if they are the same. The hash value stored in memory 34 is a result of a dynamic hashing of the data stream words stored in memory 34 that were sent by host processor 22 for programming into flash memory 24. In other words, host processor 22 executes the same hashing algorithm as flash memory 24 with respect to the data words to be programmed into flash memory 24. If the hash values stored in array 20 and memory 34 are the same, then process flow moves to process block 356, which means that the data words in the data stream have all been successfully programmed into flash memory 24. That is because a hash operation means that there is a high likelihood that the result of the hash operation is a unique number. There would only be an extremely small possibility that the hash values would ~~compare~~ be the same even though the data stream words had not been successfully programmed into flash memory 24. If the hash values are ~~substantially~~ the same at process block 354, there is a high probability that the data stream was successfully programmed into flash memory 24.

B7

Please amend the paragraph starting on page 42, line 22 as indicated below:

If process flow starts at state 404, then in order to enter the special programming mode, host processor 22 sends a series of special programming mode commands to the flash memory 24 on sequential bus cycles of bus or lines 26. When the first special programming mode command is sent by host processor 22, the command user interface 40 enters state 406, which is a special programming mode number 1 state and the output multiplexer indicates a read array signal.